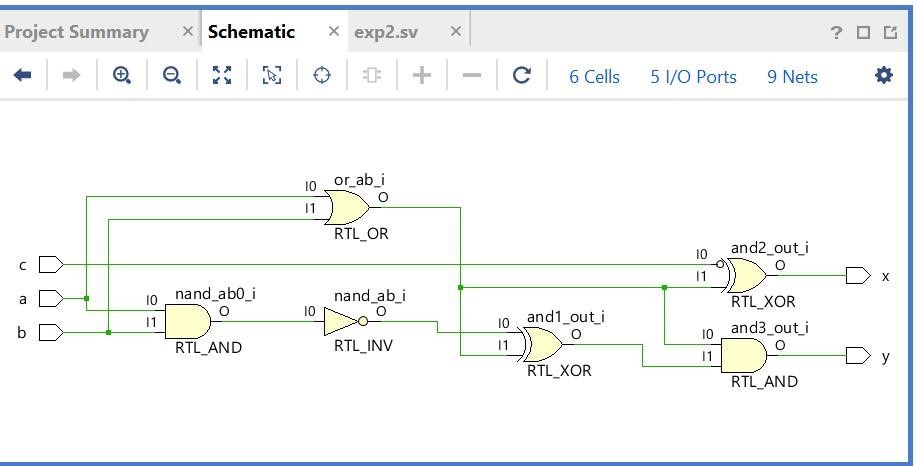
|  |  |
| --- | --- |
| **Name: Aswad jamal** | EE-272L Digital Systems Design |
| **Reg. No.: 2023-EE-84** | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual**

**DSD Lab Manual Evaluation Rubrics**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Assessment** | **Total**  **Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code  Organization  (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive  naming or code organization.  Mild to Complete understanding but not working | Proper  Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or  incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not  implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly  Implemented on FPGA or  questions related to synthesis and implementation answered. | Correctly  Implemented on FPGA and questions related to synthesis and implementation answered. |

**Schematic Diagram:**



**Task 1:**

Truth table:

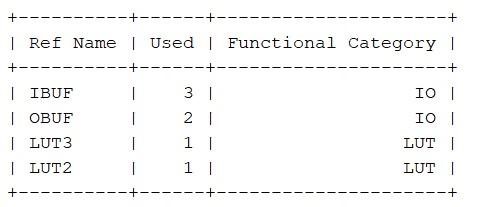
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **INPUT** |  |  | **OUTPUT** | |
| **a** | **b** | **c** | **X** |  | **Y** |
| **0** | **0** | **0** | **1** |  | **0** |
| **0** | **0** | **1** | **0** |  | **0** |
| **0** | **1** | **0** | **0** |  | **0** |
| **0** | **1** | **1** | **1** |  | **0** |
| **1** | **0** | **0** | **0** |  | **0** |
| **1** | **0** | **1** | **1** |  | **0** |
| **1** | **1** | **0** | **0** |  | **1** |
| **1** | **1** | **1** | **1** |  | **1** |

**Task 2:**



The path from a to y have max combinational delay.

**Task 3:**



2. System Verilog code for the circuit using structural modeling (using assign statements).

